

## IN THE CLAIMS:

The following listing of claims will replace all prior listings of claims in this application:

Claim 1 (Currently Amended): An adaptive computing engine, comprising: A reconfigurable input/output controller (IOC) coupled via an interconnection network to a plurality of nodes in an adaptive computing engine (ACE), wherein the coupling includes an interconnection network, the reconfigurable IOC comprising:

a programmable interconnection network;

a plurality of nodes, wherein each node included in the plurality of nodes has a fixed and different architecture that corresponds to a particular algorithmic function, and each node is coupled to one or more other nodes in the plurality of nodes via the programmable interconnection network; and  
a reconfigurable input/output (I/O) controller coupled to a first node in the plurality

of nodes via the programmable interconnection network, the reconfigurable I/O controller including:

at least one input coupled to the programmable interconnection network  
for receiving a point-to-point transfer instruction from the first node,  
for a device internal to the ACE; and

at least one output for providing a translated point-to-point transfer  
instruction to an external device.

Claims 2 - 4 (Canceled)

Claim 5 (Currently Amended): The adaptive computing engine reconfigurable IOC of claim 1, wherein [[a]] the translated point-to-point transfer instruction provides translation of a port number in the adaptive computing engine to the external device.

Claim 6 (Currently Amended): The adaptive computing engine reconfigurable IOC of claim 1, wherein [[a]] the translated point-to-point transfer instruction provides translation of an address [[from]] associated with the adaptive computing engine to an address associated with the external device.

Claim 7 (Currently Amended): The adaptive computing engine reconfigurable-IOC of claim 1, wherein the reconfigurable I/O controller further includes comprising Peek/Poke service circuitry.

Claim 8 (Currently Amended): The adaptive computing engine reconfigurable-IOC of claim 1, wherein the reconfigurable I/O controller further includes comprising memory random access circuitry.

Claim 9 (Currently Amended): The adaptive computing engine reconfigurable-IOC of claim 1, wherein the reconfigurable I/O controller further includes comprising direct memory access circuitry.

Claim 10 (Currently Amended): The adaptive computing engine reconfigurable-IOC of claim 1, wherein the reconfigurable I/O controller further includes comprising real time input circuitry.

Claim 11 (Currently Amended): The adaptive computing engine reconfigurable-IOC of claim 1, wherein the reconfigurable I/O controller further includes comprising a status line coupled to the external device for indicating an availability of services.

Claim 12 (Currently Amended): The adaptive computing engine reconfigurable-IOC of claim 1, further comprising a physical link adapter coupled to an input of the reconfigurable [[IOC]] I/O controller.

Claim 13 (Currently Amended): The adaptive computing engine reconfigurable-IOC of claim 12, further comprising; wherein the physical link adapter is coupled to coupling circuitry coupled to the physical link adapter; and a plurality of different physical connectors coupled to the coupling circuitry.

Claim 14 (Currently Amended): The adaptive computing engine reconfigurable-IOC of claim 13, further comprising; wherein the physical link adapter includes a reconfigurable finite-state machine for controlling configured to control the coupling circuitry to selectively connect a signal from a physical connector.

Claim 15 (Currently Amended): The adaptive computing engine reconfigurable-IOG of claim 1, wherein the programmable interconnection network enables communication among ~~[[a]]~~ the plurality of nodes and interfaces to reconfigure the ACE adaptive computing engine for a variety of tasks.

Claim 16 (Currently Amended): The adaptive computing engine reconfigurable-IOG of claim 1, wherein the IOG reconfigurable I/O controller runs at a clock rate associated with the programmable interconnection network clock-rate.

Claim 17 (Currently Amended): The adaptive computing engine reconfigurable-IOG of claim 1, wherein the external devices include at least one ACE adaptive computing engine, and at least one system on a chip (SOC).

Claim 18 (Currently Amended): The adaptive computing engine reconfigurable-IOG of claim 17, wherein the IOG reconfigurable I/O controller further includes status lines coupled to the SOC, the SOC being responsive to the status lines to prioritize multiple external devices.

Claim 19 (Cancelled)

Claim 20 (Currently Amended): The adaptive computing engine reconfigurable-IOG of claim 1, wherein the external device includes at least one of a host computer and a central processing unit.

Claim 21 (Currently Amended): The adaptive computing engine reconfigurable-IOG of claim 17, wherein the SOC includes at least one of a device chosen from the group comprising an ACE, a storage system, a network access system, [[and]] or a digital signal processor (DSP).